



# SD1433

## RF POWER BIPOLAR TRANSISTORS UHF MOBILE APPLICATIONS

### FEATURES SUMMARY

- 470 MHz
- 12.5 VOLTS
- CLASS C
- EFFICIENCY 60%
- COMMON EMITTER
- $P_{OUT} = 10 \text{ W MIN. WITH } 8.0 \text{ dB GAIN}$

### DESCRIPTION

The SD1433 is a Class C epitaxial silicon NPN planar transistor designed for driver applications in the 450 - 512 MHz frequency range. This device uses an emitter ballasted geometry specifically designed for optimum stable power gain, maximum efficiency and infinite VSWR.

Figure 1. Package

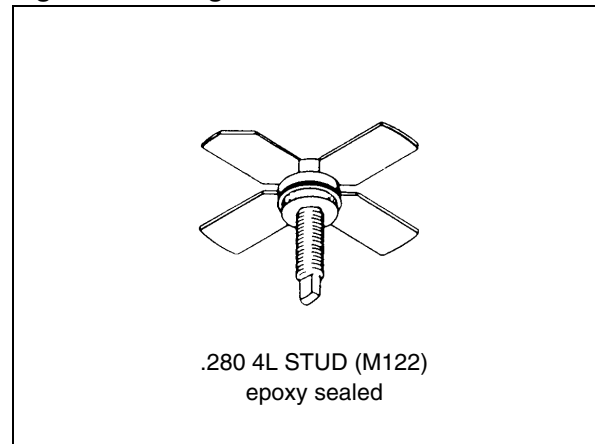


Figure 2. Pin Connection

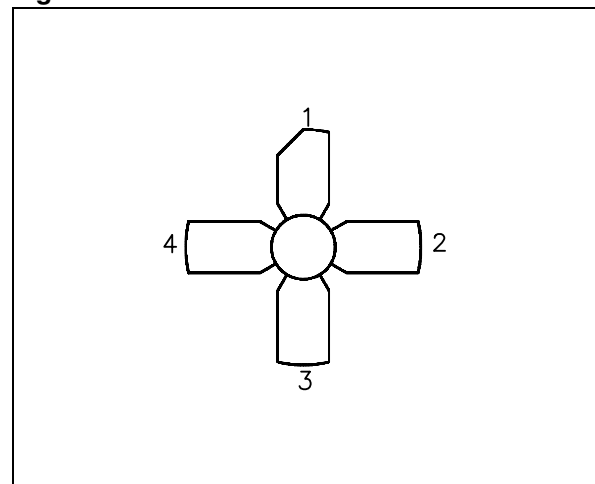


Table 1. Order Codes

Order Codes	Marking	Package	Packaging
SD1433	SD1433	M122	BLACK CARDBOARDS

**Table 2. Absolute Maximum Ratings ( $T_{case} = 25^{\circ}C$ )**

Symbol	Parameter	Value	Unit
$V_{CBO}$	Collector-Base Voltage	36	V
$V_{CEO}$	Collector-Emitter Voltage	16	V
$V_{CES}$	Collector-Emitter Voltage	36	V
$V_{EBO}$	Emitter-Base Voltage	4.0	V
$I_C$	Device Current	2.5	A
$P_{DISS}$	Power Dissipation	58	W
$T_J$	Junction Temperature	+200	$^{\circ}C$
$T_{STG}$	Storage Temperature	- 65 to +150	$^{\circ}C$

**Table 3. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Junction-Case Thermal Resistance	3.0	$^{\circ}C/W$

**ELECTRICAL SPECIFICATIONS ( $T_{CASE} = 25^{\circ}C$ )****Table 4. Static**

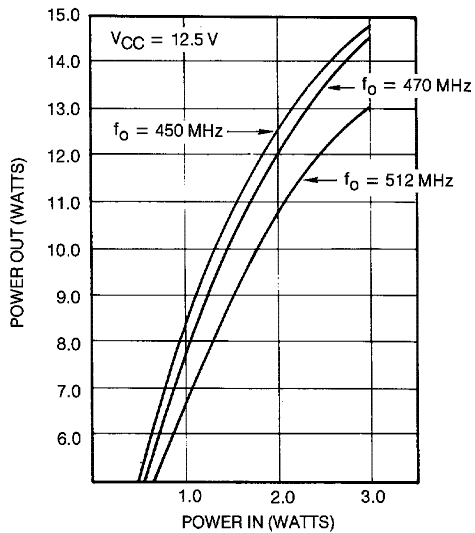
Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
$BV_{CES}$	$I_C = 25\text{ mA}; V_{BE} = 0\text{ V}$	36	—	—	V
$BV_{CEO}$	$I_C = 20\text{ mA}; I_B = 0\text{ mA}$	16	—	—	V
$BV_{EBO}$	$I_E = 10\text{ mA}; I_C = 0\text{ mA}$	4.0	—	—	V
$I_{CES}$	$V_{CE} = 10\text{ V}; I_E = 0\text{ mA}$	—	—	3	mA
$I_{CBO}$	$V_{CB} = 15\text{ V}; I_E = 0\text{ mA}$	—	—	2	mA
$h_{FE}$	$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	10	—	—	—

**Table 5. Dynamic**

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
$P_{OUT}$	$f = 470\text{ MHz}; P_{IN} = 2.0\text{ W}; V_{CE} = 12.5\text{ V}$	10	—	—	W
$G_P$	$f = 470\text{ MHz}; P_{OUT} = 10\text{ W}; V_{CE} = 12.5\text{ V}$	7	—	—	dB
$C_{OB}$	$f = 1\text{ MHz}; V_{CB} = 12.5\text{ V}$	—	19	—	pF

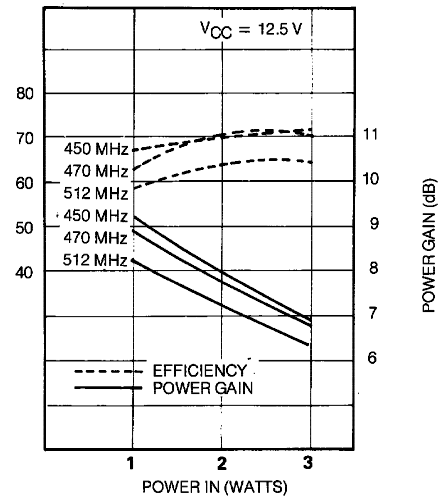
TYPICAL PERFORMANCE

Figure 3. Power Output vs Power Input



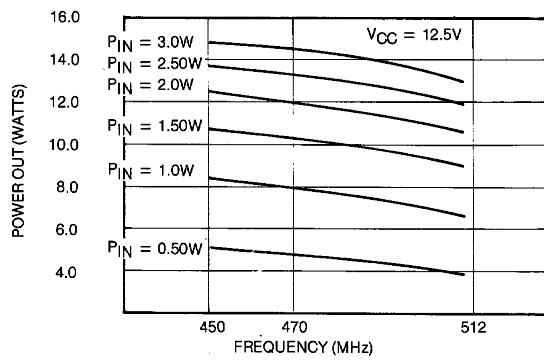
POWER OUT VS POWER IN

Figure 4. Power Gain & Efficiency vs Power Input



POWER GAIN/EFFICIENCY VS POWER IN

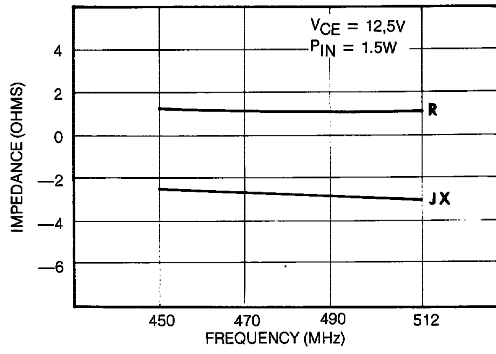
Figure 5. Power Output vs Frequency



POWER OUT VS FREQUENCY

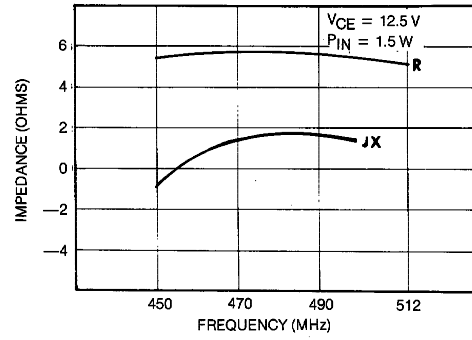
IMPEDANCE DATA

Figure 6. Typical Input Impedance



SERIES SOURCE IMPEDANCE VS FREQUENCY

Figure 7. Typical Collector Load Impedance



SERIES COLLECTOR LOAD IMPEDANCE VS FREQUENCY

Table 6. Impedance Data

FREQ.	$Z_{IN} (\Omega)$	$Z_{CL} (\Omega)$
470 MHz	$1.5 - j 2.7$	$5.7 + j 1.5$

## TEST CIRCUIT

Figure 8. Test Circuit

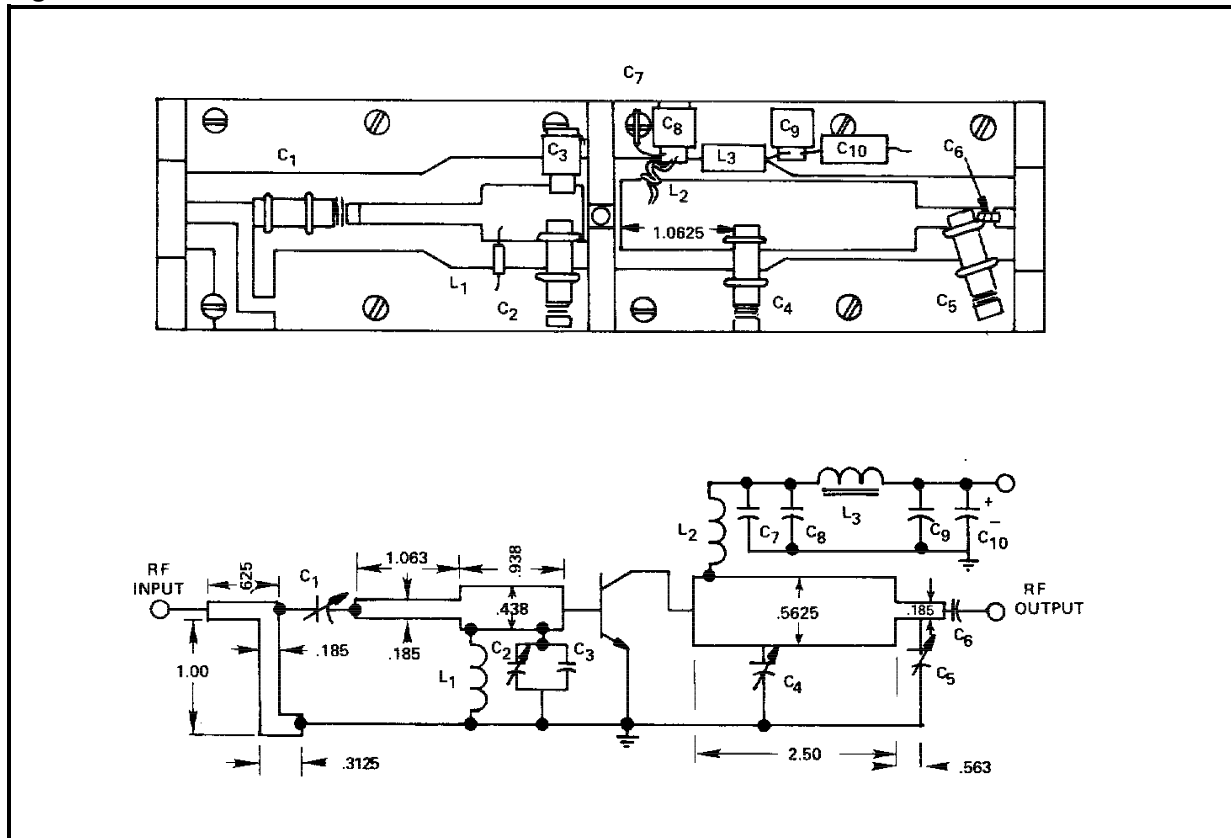


Table 7. Test Circuit

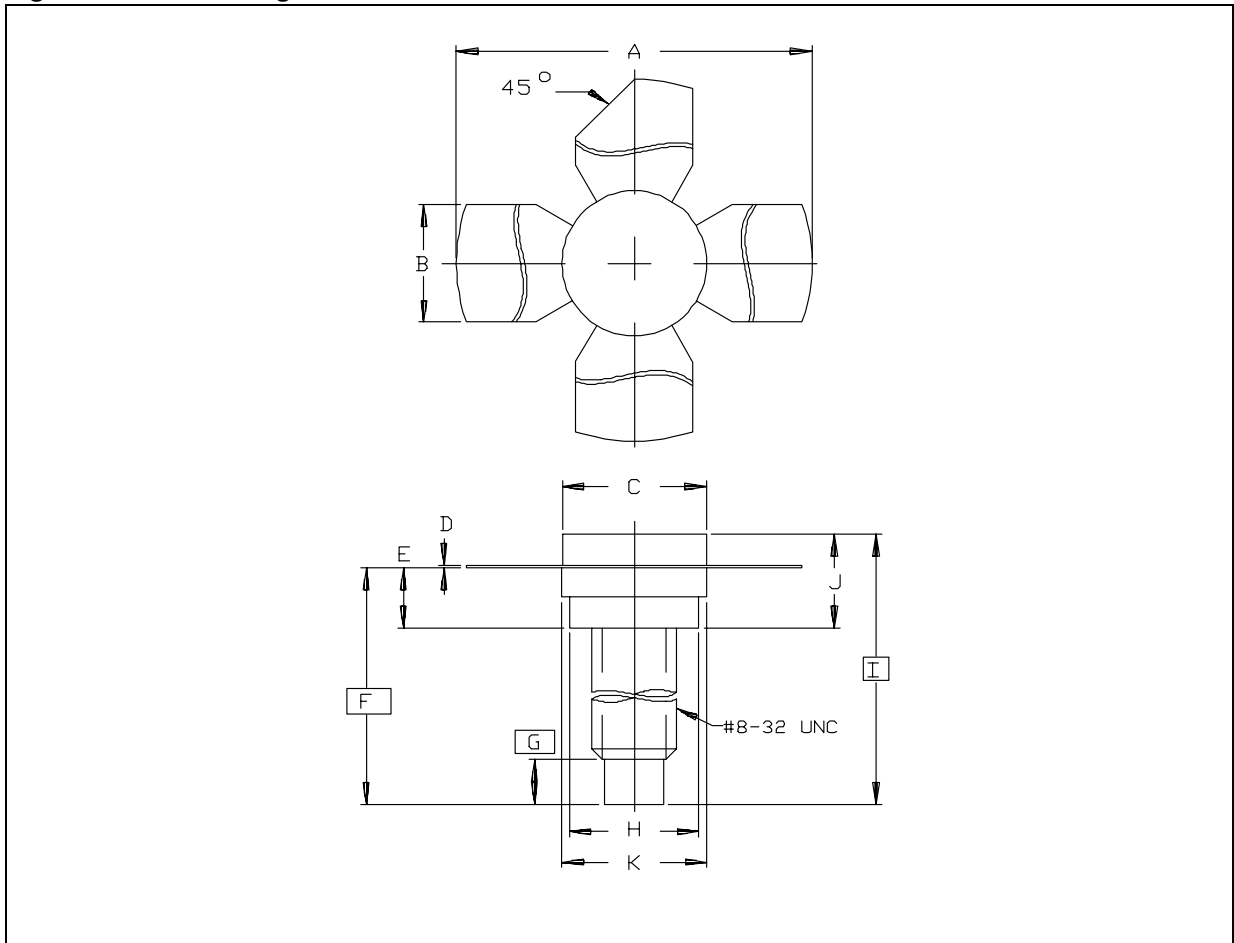
C1, C2:	0.8pF Voltronics
C3:	18pF Chip Capacitor
C4, C5:	AJ810
C6:	1000pF Chip Capacitor
C7:	0.01 $\mu$ F Disc Ceramic
C8, C9:	1000pF Unelco
C10:	10 $\mu$ F, 35V Electrolytic
L1:	0.47 $\mu$ H Molded Choke
L2:	2 Turns, #20 AWG, 1/8" I.D.
L3:	2 Turns in Ferroxcube VK200/19-4B
Board Material:	3M-K6098, 1/16" Thick

PACKAGE MECHANICAL

Table 8. M122 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.65		26.80	1.010		1.055
B	5.59		5.84	0.220		0.230
C	6.86		7.24	0.270		0.285
D	0.08		0.18	0.003		0.007
E	2.97		3.48	0.117		0.137
F		14.53			0.572	
G		3.30			0.130	
H	6.22		6.48	0.245		0.255
I		16.26			0.640	
J	4.45		5.51	0.175		0.217
K	6.99		7.24	0.275		0.285

Figure 9. M122 Package Dimensions



Note: Drawing is not to scale.

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**REVISION HISTORY****Table 9. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
November-1992	1	First Issue
28-May-2004	2	Stylesheet update. No content change.

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